



26th International Conference on Field-Programmable Logic and Applications

29th August – 2nd September 2016

SwissTech Convention Centre, Lausanne, Switzerland

<http://www.fpl2016.org>



Call for Contributions

The International Conference on **Field-Programmable Logic and Applications (FPL)** was the first and remains the largest conference covering the rapidly growing area of field-programmable logic and reconfigurable computing. During the past 25 years, many of the advances in reconfigurable system architectures, applications, embedded processors, design automation methods and tools were first published in the proceedings of the FPL conference series. The conference objective is to bring together researchers and practitioners from both academia and industry and from around the world. **FPL 2016** looks for contributions in the following areas:

Architectures and Technology

- FPGAs, GPUs and DSPs
- Heterogeneous datacentre/embedded computing
- Low power architectures
- Fault tolerant architectures
- Security and cryptography for FPGA Design
- 2.5D and 3D architectures
- Advanced on-chip interconnect technologies
- Analog and mixed-signal arrays
- Emerging technologies

Applications and Benchmarks

- Aerospace, automotive and industry automation
- Bioinformatics & medical systems

- Communications, software defined networking and Internet-of-Things
- Finance, HPC and database acceleration
- Big data analytics
- Embedded & cyber physical systems
- Signal processing and SDR
- Benchmarks for FPGA designs

Design Methods and Tools

- System-level design tools
- High-level synthesis
- Hardware / software co-design
- Logic optimization and technology mapping
- Optimizations for power efficiency
- Packing, placement and routing
- Rapid prototyping and emulation

- Testing, debugging and verification
- Open-source tools

Self-aware and Adaptive Systems

- Self-awareness in FPGA-based systems
- Self-adaptive architectures and design techniques
- Virtualization of reconfigurable hardware
- Runtime resource management
- Partial reconfiguration

Surveys, Trends, and Education

- Surveys on reconfigurable logic architectures and design techniques
- Deployment of FPGAs in new application domains
- Roadmap of reconfigurable computing platforms
- Teaching courses and tutorials

Abstract submission deadline:

20th March 2016

Paper submission deadline:

27th March 2016 (please note: **no extensions!**)

Demo night, PhD forum, workshops, and tutorials submission deadline:

8th May 2016

Notifications:

Around **15th June 2016**

Final manuscripts deadline:

3rd July 2016

Organizing Committee

General Chairs

Paolo Ienne, EPFL, CH
Walid Najjar, University of California Riverside, US

Programme Chairs

Jason Anderson, University of Toronto, CA
Philip Brisk, University of California Riverside, US

Workshop and Tutorial Chairs

Pierre-Emmanuel Gaillardon, University of Utah, US
Michael Hübner, University of Bochum, DE

PhD Forum and Demo Night Chairs

Mirjana Stojilović, HEIG-VD, CH
Yann Thoma, HEIG-VD, CH

Proceedings Chair

Walter Stechele, TU München, DE

Publicity Chair

Kubilay Atasul, IBM ZRL, CH

Local Arrangements Chair

Chantal Schneeberger, EPFL, CH

Registration Chair

Andrew J. Becker, EPFL, CH

Steering Committee

Jürgen Becker, KIT Karlsruhe, DE
Koen Bertels, TU Delft, NL
Eduardo Boemo, Univ. Autónoma de Madrid, ES
João M. P. Cardoso, Universidade do Porto, PT
Peter Y. K. Cheung, Imperial College London, UK
Martin Danek, Daiteq, CZ
Apostolos Dollas, TU of Crete, GR
Fabrizio Ferrandi, Politecnico di Milano, IT
Manfred Glesner, TU Darmstadt, DE
John Gray, Consultant, UK
Reiner Hartenstein, TU Kaiserslautern, DE
Andreas Herkersdorf, TU München, DE
Udo Kbschull, Goethe University Frankfurt, DE
Wayne Luk, Imperial College London, UK
Patrick Lysaght, Xilinx, Inc., US
Jari Nurmi, Tampere University of Technology, FI
Lionel Torres, University of Montpellier II, FR
Jim Tørresen, University of Oslo, NO