FPL 2016

Packet Processing on FPGA SoC with DPDK

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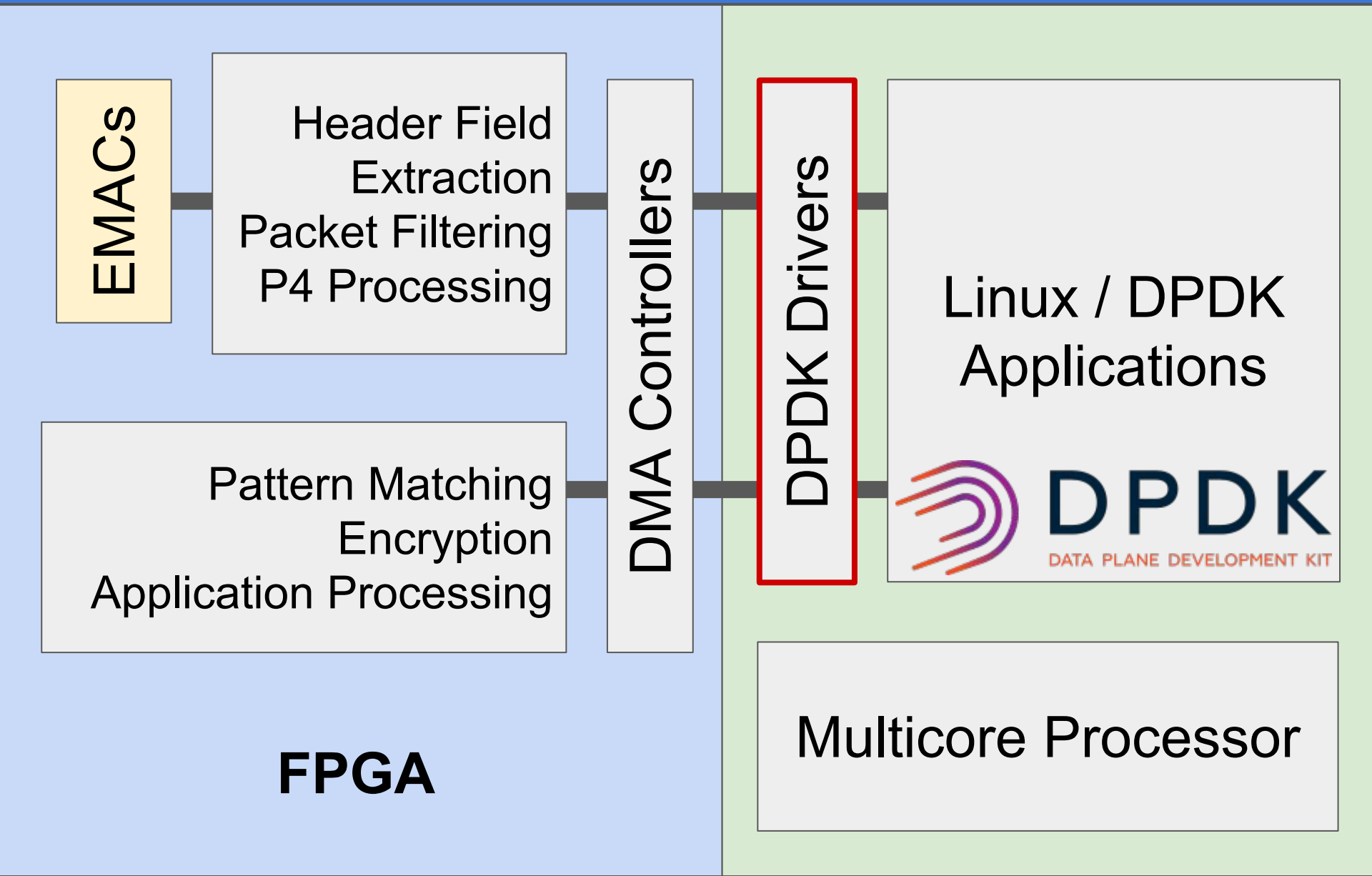
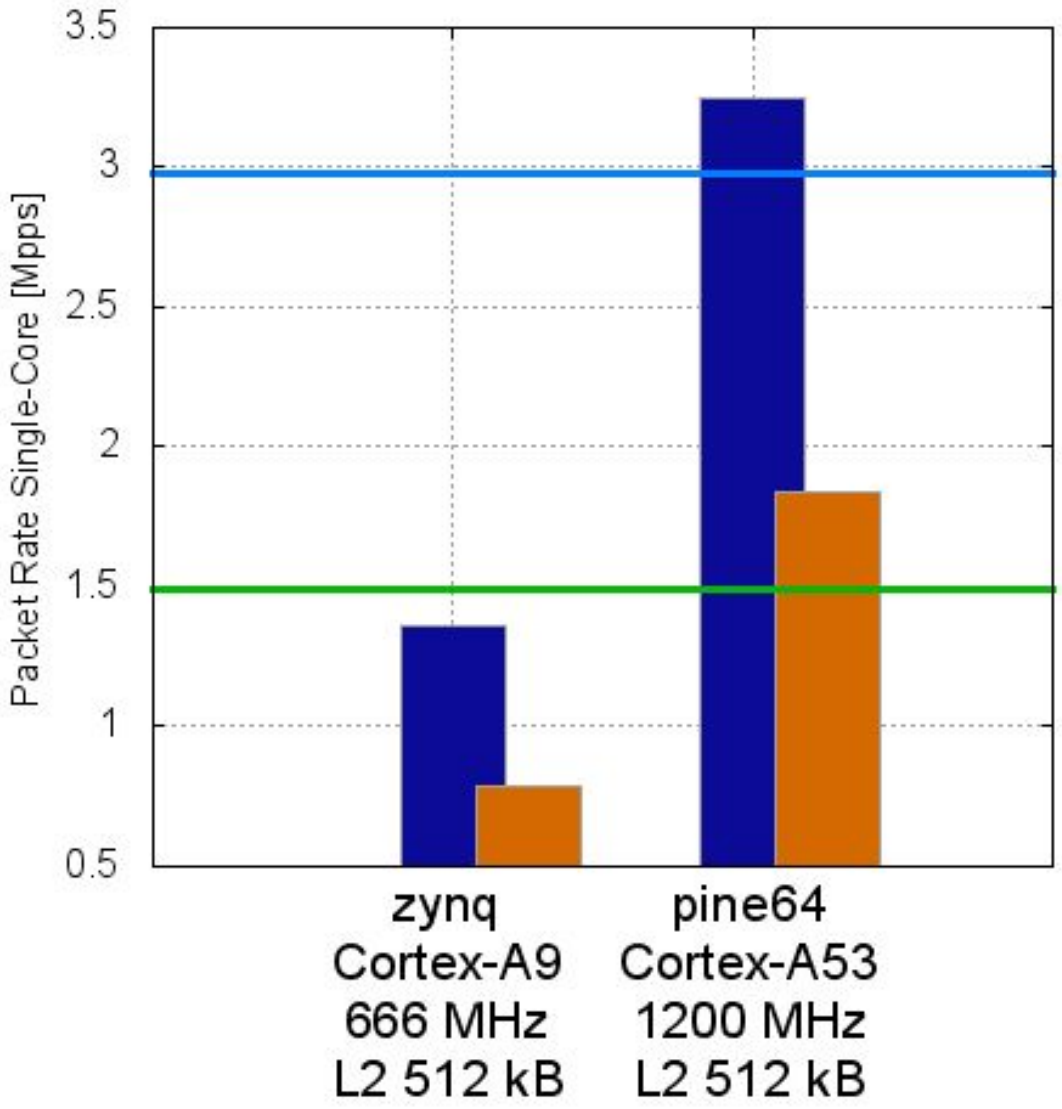
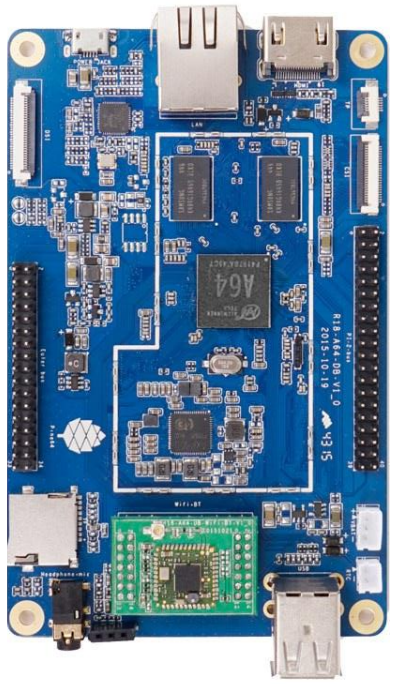
Architecture for ZynqMP



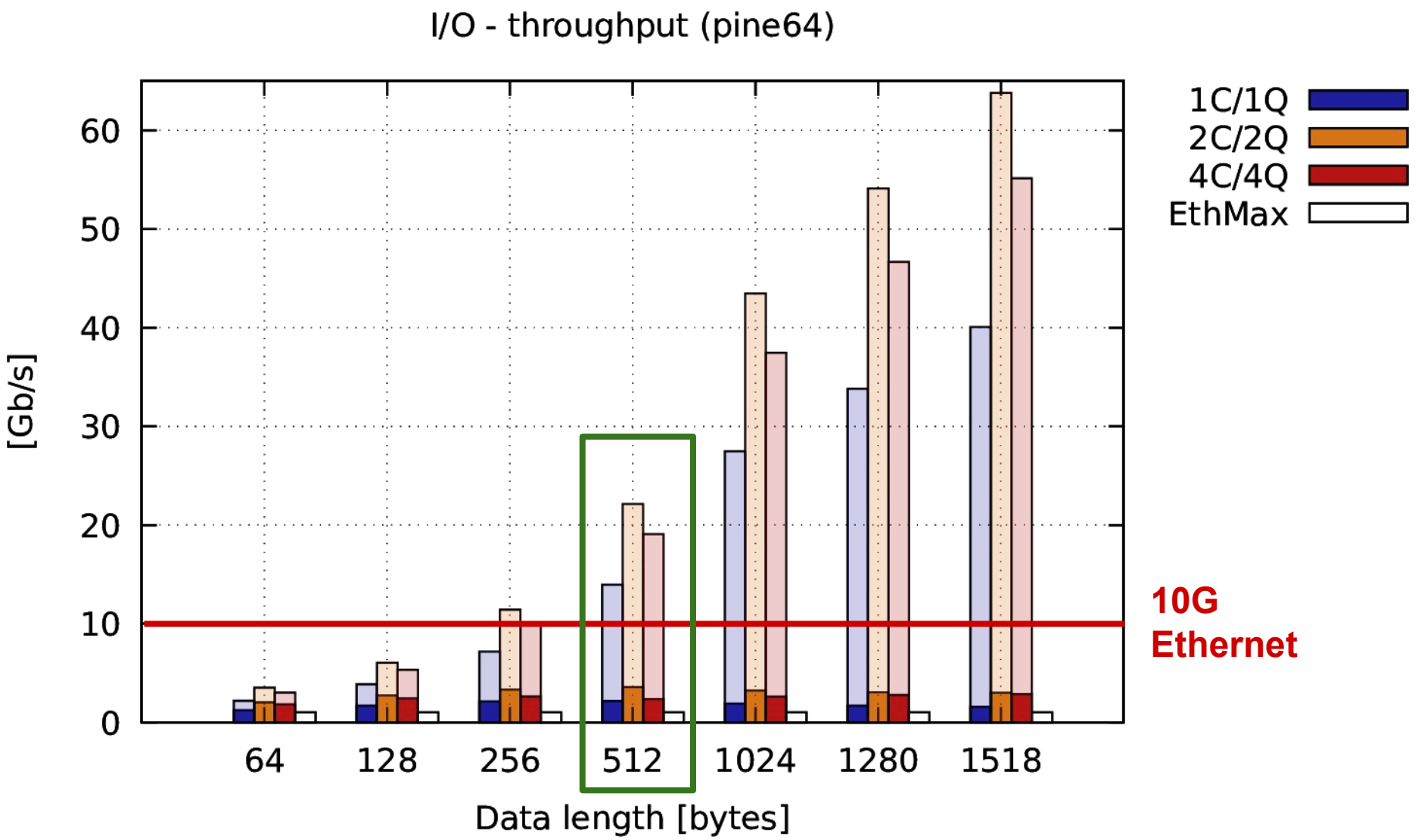
Packet rate - SW-only loopback



Pine64



Pine64 throughput (Gbps)



Thank you

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